

**METHOD AND SYSTEM FOR REDUCING POWER CONSUMPTION
IN A CACHE MEMORY**

Abstract of the Disclosure

5 A method and system are for reducing power consumption in a multi-way set-associative
cache memory. During a first clock cycle, in response to an address, an associated set is identified
in the cache memory. The address is compared to respective tag portions of blocks in the
associated set, and a signal is output in response thereto. During a second clock cycle, in response
10 to the signal indicating a match between one of the blocks and the address, a non-tag portion of the
matching block in the associated set is read, while a non-matching block in the associated set is
disabled.